Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 25, 27, 28, and 44, as follows:

Listing of Claims:

1-24. (Cancelled)

25. (Currently amended) A method of evaluating an integrated circuit having a plurality of data terminals at which data signals are received, the method comprising:

capacitively coupling a test plate integrated in the integrated circuit to a plurality of data ~~signal~~ terminals at which data signals are received;

transmitting a data signal from the test plate to one of the plurality of data ~~signal~~ terminals; and

evaluating the data signal detected by at the data ~~signal~~ terminal against a test criteria.

26. (Original) The method of claim 25, further comprising placing the remaining data terminals of the plurality in a high-impedance state.

27. (Currently amended) The method of claim 25 wherein the receiving data ~~signal~~ terminal is a first data ~~signal~~ terminal, and the method further comprises:

ceasing reception of the data signal from the first data ~~signal~~ terminal;

transmitting a data signal from the test plate to another one of the plurality of data ~~signal~~ terminals; and

evaluating the data signal detected by other data ~~signal~~ terminal against the test criteria.

28. (Currently amended) The method of claim 25 wherein the integrated circuit is formed on a semiconductor die and capacitively coupling a test plate comprises:

forming the test plate from a conductive plate layer formed on the semiconductor die; and

forming the plurality of data terminals from conductive signal pads and in proximity to the conductive plate layer, the conductive plate layer separated from the conductive signal pads by a dielectric material.

29. (Original) The method of claim 28 wherein capacitively coupling a test plate further comprises decoupling the test plate from a voltage reference and coupling the test plate to a transmitting circuit generating a test signal in response to detecting an input test signal.

30. (Original) The method of claim 25 wherein evaluating the data signal detected by the data terminal comprises:

generating a test signal applied to the test plate;

coupling the test signal detected at the data terminal to a test terminal of the integrated circuit; and

coupling test equipment to the test terminal to receive the test signal.

31. (Original) The method of claim 25 wherein the integrated circuit comprises a memory device.

32. (Original) The method of claim 25 wherein evaluating detected data signal comprises comparing the detected data signal to an expected data signal.

33-43. (Cancelled)

44. (Currently amended) A test apparatus for an integrated circuit having a plurality of capacitively coupled signal terminals to which a corresponding plurality of receivers

are coupled, the receivers generating a respective data signal in response to detecting a respective input data signal, the test apparatus comprising:

a test plate integrated in the integrated circuit to capacitively couple to the signal terminals of the integrated circuit;

a test transmitter circuit coupled to the test plate to transmit a data signal to at least one of the signal terminals through the test plate; and

a test unit coupled to the test signal terminals to evaluate the detected data signal against test criteria.

45. (Original) The test apparatus of claim 44 wherein the test transmitter comprises a buffer circuit.

46. (Original) The test apparatus of claim 44 wherein the test unit comprises test circuitry to determine the functionality of the receivers coupled to the signal terminals and the integrity of a capacitor through which the signal terminal is capacitively coupled.

47. (Original) The test apparatus of claim 44 wherein the test unit comprises test circuitry to compare the detected data signal against an expected data signal.